Amendments to the Specification:

At page 5, line 25, replace the paragraph with the following:-

--The collector electrode of transistor Q1 is AC coupled via capacitor C3 to the input of limiting amplifier stage 4, and the emitter electrode is coupled via resistor R31 to output stage 8 at the junction of resistor R29 and capacitor C16. The emitter electrode is also coupled to supply voltage +VA through resistor R6 which supplies a current source for transistor Q1. Capacitor C2 is coupled to the emitter electrode and together with resistor R31 forms a lowpass filter for filtering high frequency components and noise from SVM coil driver stage 8. High output power due to high SVM deflection signal levels in output stage 8 results in high current flow through resistor R27 which causes ~~the~~ voltage CS1 at the emitter of transistor Q1 to rise. Transistor Q1 turns on and will conduct a portion of the SVM signal at the input of limiting amplifier stage 4 through C3 and C2 to ground. This action forms a negative feedback loop which leads to a reduction in the level of the SVM deflection signal and, accordingly, the power level in output stage 8 and consequently lowers ~~the~~ voltage CS1 at the emitter of transistor Q1. Depending on the level of output power, transistor Q1 may achieve steady state operation or enter the cut off ~~stage~~ state. If output power continues to increase, the voltage at the emitter will continue to rise and transistor Q1 will accordingly divert a greater amount of the SVM signal through capacitors C3 and C2 to ground thus preventing over dissipation in output stage 8. The values of resistors R6 and R31 are chosen to control the maximum permissible temperature of the output devices in output stage 8, and the value of resistor R5 is chosen to attenuate the SVM signal level symmetrically.--

B1 cont'd

At page 7, line 8, replace the paragraph with the following:-

--When control circuitry 10 detects an SVM inhibit condition, controller 10 changes the state of the SVM ON/OFF control signal which becomes a low impedance to ground. Thus the SVM ON/OFF signal can directly ground the junction of resistors R1 and R2, or close switch SW 1, resulting in the base voltage, CS2, of transistor Q1 being pulled low. As a result, transistor Q1 turns on and conducts the SVM signal through capacitor C3 and C2 and, to a lesser extent C1, to ground thus substantially removing the SVM signal from the base of transistor Q5 and inhibiting SVM action. Once the SVM off condition terminates, the SVM ON/OFF signal reverts to a high impedance condition effectively openings switch SW 1 and allowing the voltage at the base of

B2 cont'd